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Design and Implementation of Low Power Hybrid-Type Ternary Content Addressable Memory Using Pai-Sigma Match-Line Sensing Scheme

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Abstract: A CAM compares input search data in parallel against a table of stored data and returns the address of the matching data. A BCAM stores and searches only "0"s and "1"s. A TCAM can store and search an additional state, called "don't care" so that a TCAM can perform partial matching. CAM offers high search speed in a single clock cycle, so CAMs are much faster than other search systems. Therefore CAMs are used in a wide variety of applications. Due to its parallel ML comparison 46% of power is consumed by the ML sensing structure, so TCAM is power hungry. This work proposes a Pai-Sigma ML scheme to reduce the compare power of a TCAM. The proposed ML does not incur the issues of charge sharing and short circuit current. Moreover, the switching activity of the search lines of a TCAM with the proposed MLs is low. A 3x3-bit Hybrid-type TCAM with the Parallel Pai-Sigma MLs is implemented to demonstrate the low-power feature. Results show that the compare power of the Hybrid-type TCAM can achieve 60% energy reduction compared with the conventional NOR-type TCAM. Also, the power consumption of the Hybrid-type TCAM is only 9.3962 µW.

Keywords: **Ternary Content Addressable Memory (TCAM), Binary Content addressable Memory (BCAM), Random Access Memory, NOR-type TCAM, NAND-type TCAM, Hybrid-type TCAM, Match-line (ML), Search-line (SL), Bit-line (BL).**

I. INTRODUCTION

High speed networks are gaining huge popularity in bandwidth hungry real time applications such as packet classify and forwarding. The internet is a mesh of routers and switches, which process data packets and forwards them towards their destination. Each router maintains a routing table and forwards incoming packets based on the information stored in the routing table. As the capacity of routing table increases the speed of table lookup drops off. Software methods such as radix tree and hash function for lookup operation are slow relatively; they do not scale well with table size. Therefore, software methods are now being replaced by hardware solutions to meet performance requirements. An efficient hardware solution to perform table lookup is the CAM. CAM is an outgrowth of RAM. It supports both search and store operations. CAM stores a number of data words and perform parallel comparison of search data words with all the stored entries. If a match is found, the corresponding memory location is retrieved. In case of multiple matches, a priority encoder resolves the highest priority match. CAMs are divided into BCAM and TCAM. A BCAM can only search and store either '0' or '1'. Thus, BCAMs are suitable for applications that require only exact match searches. But, TCAMs can store and search ternary state called 'X' i.e. don't care. It can be used as a wild card entry to perform partial matching. However, high power dissipation is one of major disadvantages of the TCAM.

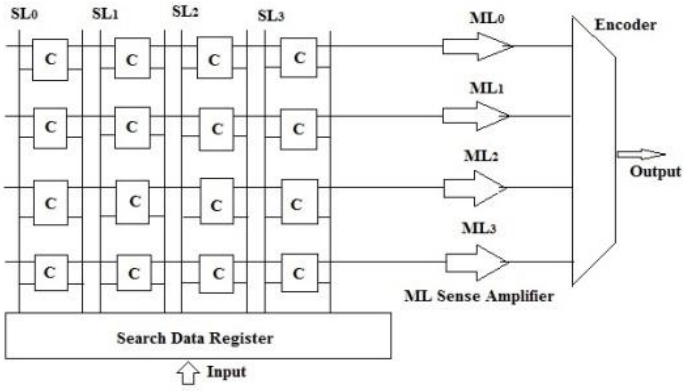


Fig.1 Basic Schematic of CAM [1].

The fig.1 Shows 4x4 CAM consists of CAM core cells, horizontal MLs and vertical SLs, ML sense amplifier (MLSA) and encoder. The input search data is applied to search data register which is broadcasted onto the SLs. MLs are pre-charged to high equal to supply voltage. Each cell is connected to ML which indicates whether the search data and stored data are identical. The MLSA then detects whether its ML has a matching condition or Mismatch condition. If the data is identical, it is called Match condition otherwise the condition is Mismatch. If the condition is Mismatch then the ML will be pull down. The MLSA are fed to an encoder that generates a binary match location to its encoded address corresponding to the ML of highest priority.

II. CORE CELL

A TCAM Has Three Major Components

(a) 8T BCAM cell that contains the stored data implemented using the cross coupled inverter and compare unit is implemented using pass transistor logic which compares the stored data with search data. Depending on the different applications, the compare unit can be implemented as XOR or XNOR functions.

(b) 6T SRAM cell is used for storing mask bit to indicate whether TCAM is in don't care state or not. This is called Mask bit cell. TCAM state is determined by Mask bit (Mi). If Mi = 0, TCAM cell is in don't care state in which there is always match regardless of the comparison result. Such condition is called Wild Match. If Mi = 1, in case of search data and stored data are identical it is called Normal Match otherwise it is Mismatch Condition.

(c) Evaluation logic is used to either pull down the ML or not. If the condition is Match then it retains the ML to logic high otherwise it is pull down to ground.

TCAM has three basic operations: write, read and compare operations. The NMOS access transistors and BLs which are used to read and write the SRAM storage bit. The SLs are used to broadcast search data and MLs are used to indicate the Match or Mismatch condition. BLs is used for performing read and writes operations.

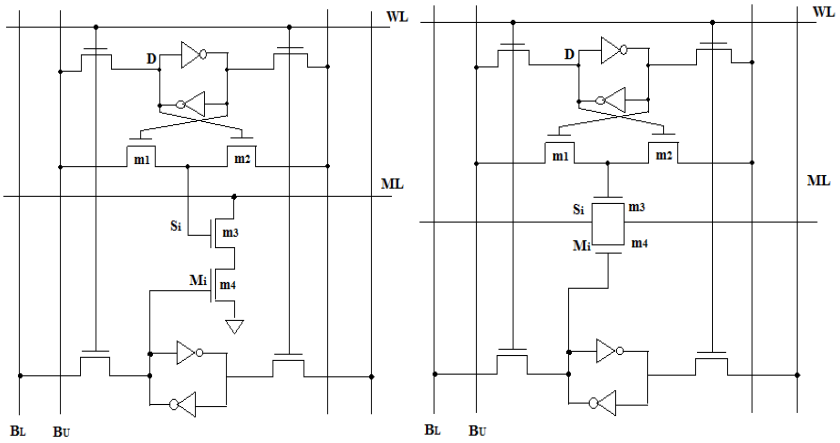


Fig.2 Schematic of (a) NOR-type TCAM cell (b) NAND-type TCAM cell [30].

A. NOR-Type TCAM

Fig. 2(a) depicts NOR-type TCAM cell which usually implements XOR-type CAM cell and the pull down transistors of TCAM cell are arranged in NOR-type. During compare operation of TCAM in pre-charge phase, the ML is initially pre-charged to high. Transistors m3 and m4 are connected in series to indicate NOR-type cell, the status of ML is determined by the value of all four NMOS transistors m, m2, m3 and m4. In evaluation phase, if Mi = 0 ML remains in logic high state otherwise ML will be discharged to ground if output is in Mismatch State. The pull down path is very short, in case of a mismatch the ML is discharged to ground quickly compared to NAND-type TCAM hence it provides best compare performance. But at the cost of high power consumption as more power is dissipated in ML switching contributed by drain capacitances to ML.

B. NAND-Type TCAM

Fig. 2(b) depicts NAND-type TCAM cell which usually implements XNOR-type CAM cell and the pull down transistors of TCAM cell are arranged in NAND-type. The ML is initially pre-charged to logic high, and discharged to 0 only when all CAM cells are matched. Because the load capacitance of ML is small and only one ML is discharged to 0 during search, hence the power consumption is minimal. As the pull down path is too long, such that the ML discharge is very slow in case of a Match. Thus, NAND-type TCAM consumes low power at cost of low performance.

C. Hybrid-Type TCAM

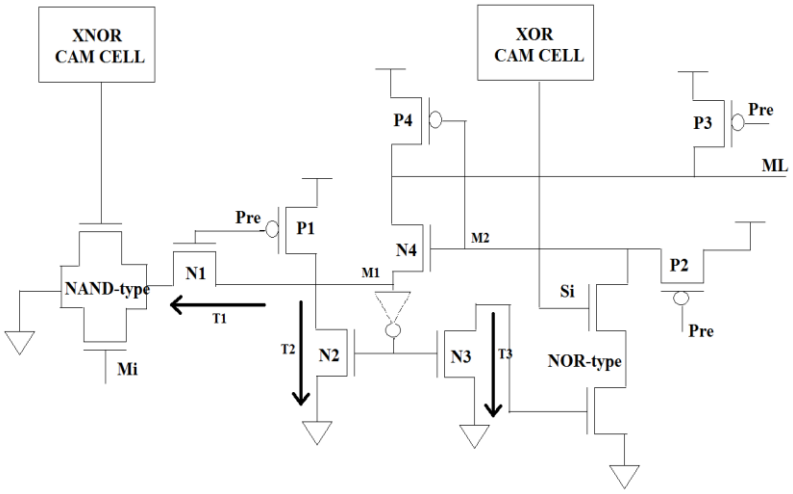


Fig.3 Schematic of Hybrid-type TCAM cell [12].

Fig. 3 depicts Hybrid-type TCAM cell which achieves the best performance with low power consumption. When CAM performs compare operation, all the NAND MLs are activated. But only the NOR MLs with the corresponding NAND MLs generating a Match result are activated. Since the switching power of the NAND ML is less and only a small amount of NOR MLs are activated, the compare power of the CAM with NAND-NOR ML is better than that of the NAND ML. As shown in the fig. 3 the CAM cell is implemented as XNOR-type and their pull-down transistors are arranged in the NAND-type. The NAND-type block is connected to the ground only when all the CAM cells are matched. The XOR-type CAM cell is implemented and their pull down transistors are placed as NOR-type. The NOR-type block is disconnected from the ground only when all the CAM cells are matched.

During pre-charge phase, all the MLs are initially pre-charged to logic high and during the evaluation phase only those MLs which will be in mismatch state are pull down to ground.

(a) Pre-charge Phase: In this phase, the control signal Pre will be low. Thus ML is initially pre-charged to high. Because the pull down path T1, T2 and T3 are disconnected by N1, N2 and N3 transistors respectively both M1 and M2 nodes are pre-charged to high via P1 and P2. Due to no paths to the ground, it is unnecessary to discharge all the BLs to ground to prevent the unexpected short circuit during the pre-charge phase.

(b) Evaluation Phase: In this phase, the control signal Pre is asserted high and the search data have to be loaded on the BLs to start the matching process. This is called match evaluation phase. When both NAND-NOR type blocks are matched it is called normal Match. If the case is mismatch in NAND-type block then one of the NMOS transistor is

turned off that disconnects the pull down path T1 from the ground. Therefore, node M1 retains high that turns off the tail transistor N2 and N3 to disconnect the pull down path T2 and T3 irrespective of the condition in NOR-type block node M2 will be still high to turn on N4. Because the path T1 and T2 are disconnected from the ground, the ML would retain logic high as in the initial phase. In case of Match in NAND-type block and Mismatch in NOR-type block, then NMOS transistors of NAND-type block are turned on that connects the path T1 to ground. Therefore, node M1 is discharged to ground that turns on the tail transistors N2 and N3.

III. EXISTING METODOLOGY

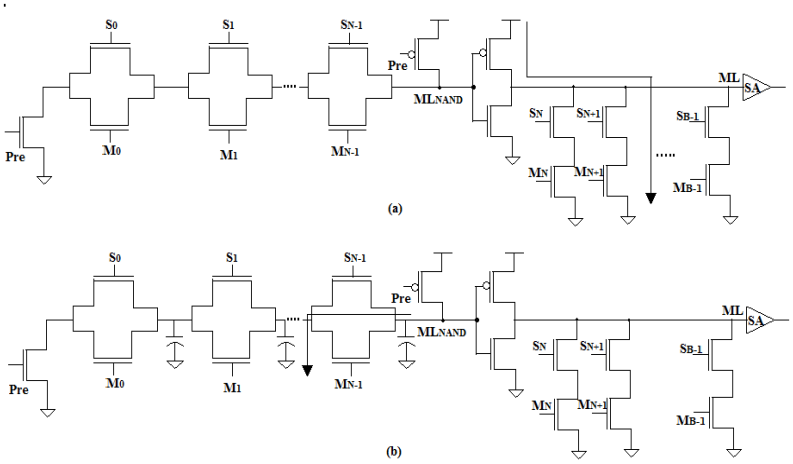


Fig.4 Schematic of (a) Short circuit current (b) the charge sharing in a ML [30].

As shown in fig. 4(a) short circuit current occurs due to switching activity, since there will be a finite rise and fall time for both PMOS and NMOS transistors. During transition from OFF to ON, both transistors will be on for a period of time in which current will find a path directly from VDD to ground creating a short circuit current. Hence short circuit power dissipation increases with rise and fall time of the transistor. It consumes 20% of the total power dissipation. As shown in fig. 4(b) the charge sharing problem occurs when charge is stored at the output node in the evaluation phase which gets shared among the output or junction capacitors. The Charge sharing degrades the output voltage level and even causes erroneous result.

A. PAI-SIGMA ML STRUCTURE

Fig. 5 shows the transistor-level diagram of the proposed Pai-Sigma ML scheme, where only the comparison logic of the TCAM cells is shown. The Pai segment realizes NAND function that is $\prod_{i=0}^{p-2}(Si + Mi)$. The Sigma segment realizes NOR function that is $\overline{\sum_{j=p}^{n-1} \overline{Sj} * \overline{Mj}}$. The $Cell_{(p-1)}$ is merged with the interface logic between the Pai segment and Sigma segment. Fig. 6(c) shows the timing diagram of control and match signals of the Pai-Sigma ML when a Compare operation is performed. For the Pai segment, i.e., $Cell_0$ to $Cell_{(p-2)}$, the comparison logic of each cell is comprised of two NMOS transistors in shunt and two PMOS transistors in series. Each Pair of PMOS and NMOS transistors is controlled by Si and Mi. For the Sigma segment, i.e., $Cell_p$ to $Cell_{(B-1)}$, the comparison logic of each cell is two NMOS transistors in series. The comparison logic of the $Cell_{(p-1)}$ is mixed with the interface logic. In the pre-charge phase (pre = 0), for the Pai segment all internal nodes (i.e., I0, I, …, Ip-3, ML_{nand}) between two adjacent comparison logics can be charged to VDD or VDD- Vth regardless of the states of Si and Mi. The reason is that if (Si,Mi) = (1,1), (1, 0), or (0, 1), then Ii+1 = Ii. If (Si,Mi) = (0,0), then the PMOS transistors controlled by Si and Mi are turned on and the corresponding internal node Ii is pre-charged to logic 1. Therefore, the SLs of the cells from $Cell_0$ to $Cell_{(p-2)}$ do not need to be reset to guarantee that all internal nodes can be charged to logic 1. This can eliminate the dynamic power for resetting the SLs. The node ML_{nand} can be charged to VDD through the pre-charge PMOS transistor. This guarantees that no DC current exists in the interface logic. In the evaluation phase (Pre = 1), if both Si and Mi for $0 \leq i \leq$ p-2 are not logic 0, i.e., the search result is match, then ML_{nand} = Ip-3 = Ip-4. If any (Si,Mi) of the cells from Cell0 to Cellp-2 is (0, 0), i.e., the search result is mismatch, then the corresponding PMOS transistors are turned on and the corresponding internal node Ii+1 is pre-charged to logic 1. Then, the logic 1 is propagated to upstream internal nodes (Ii+2, Ii+3, …, ML_{nand}) through the NMOS pass transistors. To overcome with the issue of short circuit current, the proposed Pai-Sigma ML uses a static CMOS gate to cascade the NAND ML and the NOR ML.

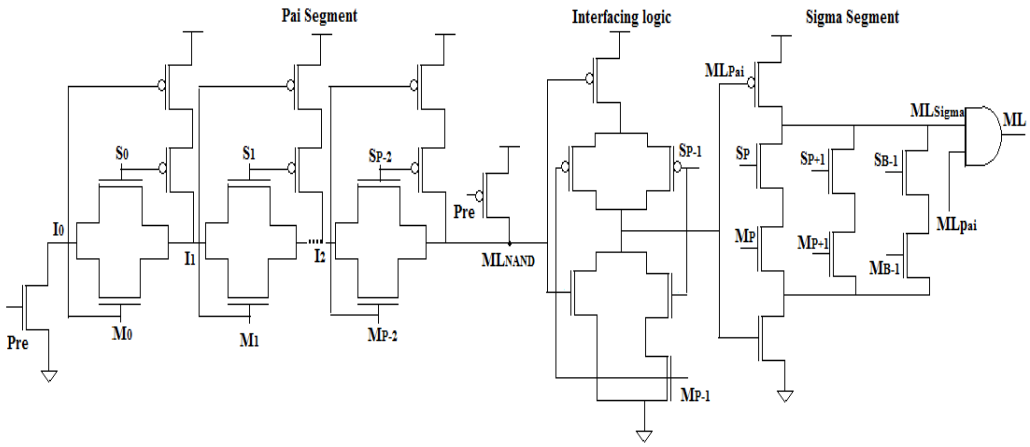


Fig.5 Schematic of Pai-Sigma ML scheme [30].

Table I

ML_{Nand}	ML_{Pai}	ML_{Sigma}	ML
1	0	1	0(Mismatch)
0	0	1	0(Mismatch)
0	1	0	0(Mismatch)
0	1	1	1(Match)

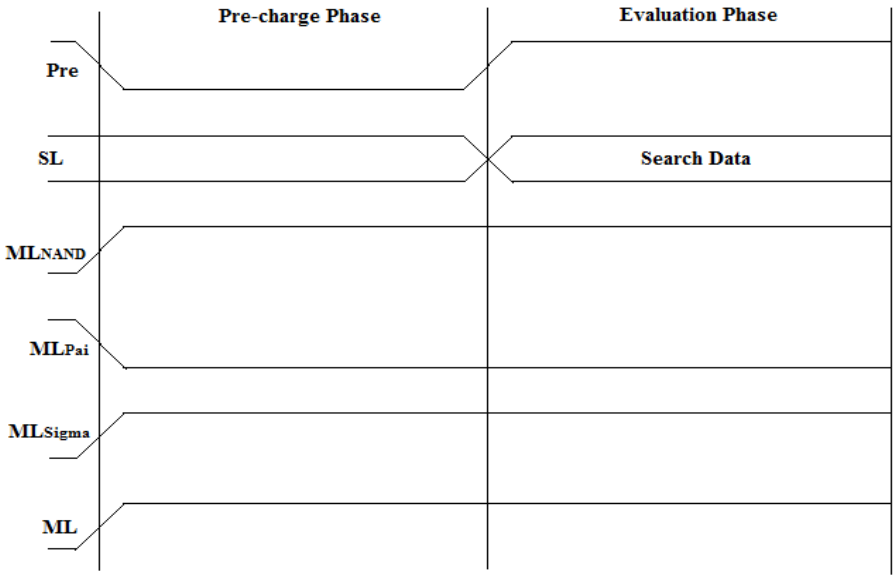


Fig.6 (a) Truth table of ML (b) Timing diagram of ML structure [30].

As Fig. 5 shows, the inputs of the static CMOS gate which consists of ML_{nand}, $\bar{M}$p-1and $\bar{S}$p-1. The static CMOS gate also serves the comparison logic of the $Cell_{p-1}$. Therefore, if the search result of $Cell_0$ to $Cell_{p-1}$ is match, the interface logic generates logic high at ML_{Pai} node. The pre-charged PMOS of the NOR ML will be turned off. If the search result of NOR ML is miss, then no short-circuit path exists. The final search result of a ML is the ML. Fig. 6(b) shows the truth table of ML with respect to the ML_{nand}, ML_{Pai} and ML_{Sigma}.

B. PARALLEL PAI-SIGMA ML STRUCTURE

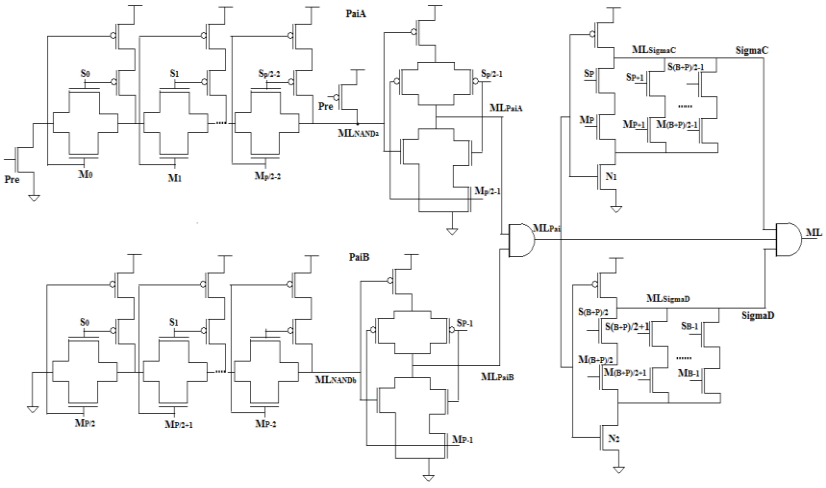
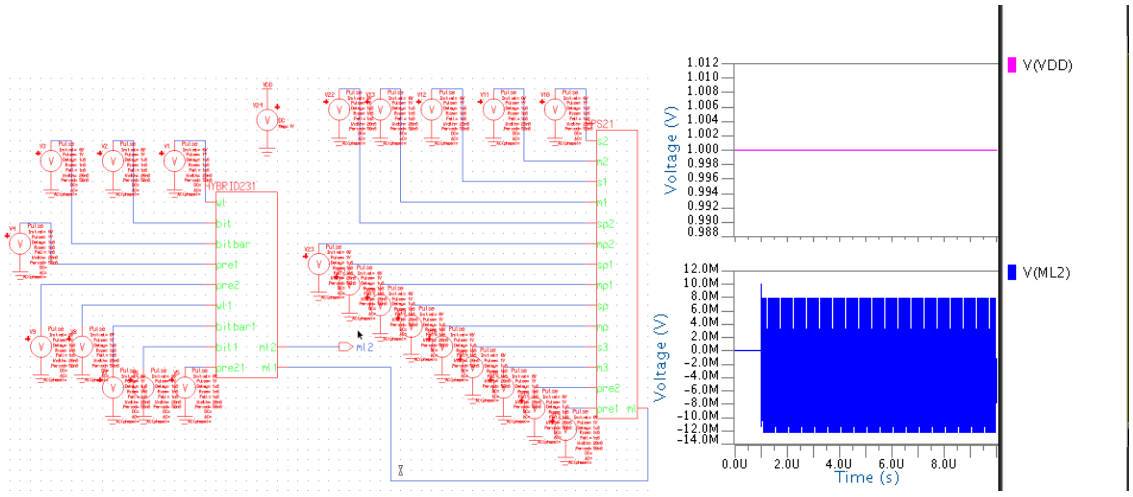


Fig.7 Schematic of Parallel Pai-Sigma ML scheme [30].

The two sub-segment Pai segment is selected to realize a Parallel Pai-Sigma ML (P^2SML) scheme. The Sigma segment is also partitioned into two sub-segments to reduce the delay and power consumption. Fig. 7 shows the proposed Parallel Pai-Sigma scheme, where the Pai segment is separated into the Pai_A and Pai_B and the Sigma segment is separated into the $Sigma_C$ and $Sigma_D$. The pre-charge operation of the $Sigma_C$ and $Sigma_D$ is controlled by the result of ML_{Pai}. If the comparison result of the Pai segment is match, the ML_{Pai} = 0 and the MLs of $Sigma_C$ and $Sigma_D$ are pre-charged to VDD. The ML_{Pai} is the AND of ML_{PaiA} and ML_{PaiB}. Thus, if either ML_{PaiA} or ML_{PaiB} is at logic 0 in pre-charge phase or a miss result, then the ML_{Pai} is 0 and the MLs of $Sigma_C$ and $Sigma_D$ can be pre-charged to VDD. Therefore, only a pre-charge control circuit is implemented in the Pai_A segment, which can guarantee the ML to be set to logic 0 in the pre-charge phase. This can also reduce the power consumption contributed by the pre-charge signal. If a Compare operation is performed, the pre-charge control signal Pre is set to 0 and the ML_{PaiA} becomes logic 0. Then, the match- lines of $Sigma_C$ and $Sigma_D$ are pre-charged to VDD in the pre-charge phase. In the evaluation phase, if the comparison result of the Pai segment i.e., from $Cell_0$ to $Cell_{p-1}$ is match, then the ML_{PaiA} and ML_{PaiB} are logic 1. The state of ML_{Pai} thus becomes logic 1. Therefore, the NMOS transistors N1 and N2 are turned on and the MLs of $Sigma_C$ and $Sigma_D$ are in the evaluation phase. If the comparison results of $Sigma_C$ and $Sigma_D$ are also match, then the results of the ML_{SigmaC} and ML_{SigmaD} are logic high and the ML is logic high. If the comparison result of the Pai segment is mismatch, then the charge in the Sigma segment is not discharged, i.e., at logic high state.

IV. PROPOSED PAI-SIGMA ML STRUCTURES FOR HYBRID TCAM



(a) **(b)**

Fig.8 Schematic and waveform of Hybrid Parallel Pai-Sigma ML scheme.

Hybrid-type TCAM lowers the power consumption and provides high performance. And parallel Pai-Sigma ML sensing scheme overcomes the short circuit current and charge sharing problem which is the main cause for power consumption. By using Hybrid-type TCAM with parallel Pai-Sigma structure the performance can be enhanced and power consumption can be lowered compared to NOR-type TCAM. In pre-charge phase, initially Pre control signal is set to logic zero state. As all SLs does not get activate at a time so there is no need to reset unnecessary SLs. Hence no DC current exists in the interface logic. As Pai segment acts as pre-charge control circuitry switching activity is reduced. In evaluation phase, the ML value of both sigma and Pai remains at logic high state, the value of output does not get degraded hence charge sharing is reduced. And also pre-charge PMOS of NOR ML block will be off for mismatch state only the corresponding NAND ML with match state gets activated which reduces the power to greater extent. As shown in fig. 8(b), the transient behavior of parallel Pai-Sigma ML with Hybrid-type TCAM is depicted. With the supply voltage of 1V with search data 5V and stored data 5V, the data is identical hence the output is normal match therefore output is logic high state.

V. RESULT ANALYSIS

A. SIMULATION RESULT

The number of bits of the Pai ML has a great influence on the speed and power of the Compare operation. To design a low-energy TCAM, the product of the speed and power must be minimized. So the product of the power and delay is minimal when the value of p is small. For example, an 8-bit Pai segment can be implemented by 1, 2, 4, or 8 sub-segments and then the comparison results of those sub-segments are evaluated by using interfacing logic circuits. As two sub segment Pai segment is selected to realize parallel Pai-Sigma ML scheme the delay and power consumption is reduced. For experimental study 3X3 bit P^2SML Hybrid-type TCAM is implemented using 0.18µm CMOS process technology. The measured power consumption of the Hybrid-type TCAM is 9.3962µW which is less compared to NOR-type TCAM i.e. about 30.8467µW. The numbers of MOS used are 1813734 with number of nodes 451, with number of components 550 and the average iterations are equal to 3.660664. And also the power consumption of NAND-type cell which is nearly 48.894µW with the supply voltage of 1.2V.

B. COMPARISION RESULT

Table.II Performance Comparision

ML sensing schemes	Power (µW)	Delay(ns)	Charge sharing	DC path in ML	Technology(µ m)	Applicatio n	Result
AND CAM [11]	56.21	2.1	Y	N	0.18	General	Measured
PNN CAM [9]	1200	3.8	Y	Y	0.25	General	Measured
Tree-style TCAM [5]	245.9	1.52	Y	N	0.18	Specific	Measured
P^2SML [30]	280	1.99	N	N	0.18	General	Measured
Hybrid TCAM P^2SML*	9.3962*	1.34*	N	N	0.18	General	Measured

Table II summarizes the comparison results of the proposed low power TCAM and existing low power TCAMs. The TCAMs reported in [9], [11] and [30] are designed for general application. Thus, the specific low power design techniques can be used to reduce the search energy. For example, the power consumption reported in [5] is 245.9µW. For general applications, the proposed Hybrid-type TCAM with Parallel Pai-Sigma MLs has the lowest power consumption. Also, the issue of charge sharing induced by the NAND-type ML is eliminated by the specific Pai circuit in the proposed P^2SML scheme. The issue of DC path existing in the interface between the NAND-type ML and NOR-type ML is also resolved by using the Hybrid-type ML. In paper [8], although the issues of charge sharing and DC path do not exist by

adding an additional timing control signal connecting to the NOR-type ML, this consumes additional power. Therefore, the total power consumption is larger than that of P^2SML scheme. In [11], even though the AND-type ML scheme can be used for BCAM and TCAM, the search energy is measured from BCAM. Clearly, if the TCAM is considered, the energy will be larger. Hence the proposed Hybrid-type P^2SML costs only 40% of power against NOR TCAM.

VI. CONCLUSION

In this paper a low power Hybrid-type TCAM using parallel Pai-Sigma ML sensing scheme is designed and implemented which does not incur the issues of charge sharing and DC path. The switching activities of the SLs are reduced. The proposed low power hybrid-type TCAM with P^2SML is implemented using 0.18µm CMOS technology. Results show 60% power reduction compared to the existing P^2SML [30] NOR-type TCAM. Also, the power consumption is about 9.3962µW.

VII. ACKNOWLEDGEMENT

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